## **Amendments to the Claims:**

Cancel claims 5, 6, 11, 15, 24, and 26. This listing of claims will replace all prior versions, and listings of claims in the application:

## **Listing of Claims:**

1

2

3

4

1

- 1 1. (Original): A processor operable from an M-bit instruction set or an N-bit 2 instruction set, where M and N are integers, and M is less than N, comprising: a memory unit for storing at least first and second instruction streams respectively 3 4 comprising N-bit instructions and M-bit instructions 5 an execution unit operable to receive execution signals to execute the N-bit 6 instructions; a decode unit coupled to the memory unit and to the execution unit to receive and 7 8 decode the first and second instruction streams from the memory unit to produce therefrom the 9 execution signals, the decode unit including a translation unit for receiving each of the M-bit 10 instructions to translate each of a first group of the M-bit instructions to a corresponding one of 11 the N-bit instructions, and to translate each of a second group of the M-bit instructions to two or 12 more N-bit instructions for decoding by the decode unit.
  - 2. (Original): The processor of claim 1, wherein each of the M-bit and N-bit instructions are stored in the memory unit at locations identified by memory addresses having at least one bit position set to a first state to identify a memory address of an M-bit instruction and a second state to identify a memory address of an N-bit instruction.
- 3. (Original): The processor of claim 2, the N-bit instruction stream including at least one N-bit branch instruction, the decode unit operating to execute the N-bit branch instruction to switch from executing N-bit instructions to executing M-bit instructions.
  - 4. (Original): The processor of claim 1, where N is equal to 2M.

Appl. No. Unassigned Amdt. dated August 19, 2003 Preliminary Amendment

1	5. (Canceled)						
1	6. (Canceled)						
1	7. (Original): A processor unit, including						
2	a memory for storing a plurality of instructions, including M-bit instructions and						
3	N-bit instructions where M and N are integers and M is less than N, each instruction being stored						
4	at a memory location identified by a memory address, each memory address having a bit position						
5	set to a first state for M-bit instructions and to a second state for N-bit instructions;						
6	an instruction flow control unit for retrieving the instructions from the memory						
7	for controlling execution of the retrieved instructions, the instruction flow control unit including						
8	a translation unit operable to receive ones of the M-bit instruction for translation to a sequence of						
9	two or more N-bit instructions.						
1	8. (Original): A microprocessor, comprising:						
1							
2	a memory element containing a plurality of M-bit instructions and N-bit						
3	instructions where M and N are integers and M is less than N;						
4	an instruction fetch unit coupled to the memory element for retrieving selected						
5	ones of the M-bit instructions or N-bit instructions therefrom, the instruction fetch unit including,						
6	a translator unit for translating each of the M-bit instructions fetched from the						
7	memory element into a sequence of one or more N-bit instructions; and						
8	a decode unit coupled to the memory element and to the translator unit for						
9	receiving each of N-bit instructions fetch from the memory element and each of N-bit						
10	instructions from the translator unit for decoding such N-bit instructions.						
1	9. (Original): The microprocessor of claim 8, including at least one target						
2	register for holding a target address, the plurality of N-bit instructions including a prepare target						
3	instruction that, when executed by the microprocessor, loads the target address in the target						
4	register.						
•							

Appl. No. Unassigned Amdt. dated August 19, 2003 Preliminary Amendment

i	10. (Original): The microprocessor of claim 9, wherein the pluranty of N-bit						
2	instructions includes a BLINK branch instruction operating to use the target address in the target						
3	register to branch to cause an M-bit target instruction or an N-bit target instruction to be fetched						
4	from the memory element for translation or decode, respectively.						
1	11. (Canceled)						
1	12. (Original): The microprocessor of claim 9, wherein the target address						
2	includes a bit position set to a first state to identify an M-bit target instruction.						
1	13. (Original): The microprocessor of claim 12, wherein the bit position is set						
2	to a second state to identify an N-bit target instruction.						
1	14. (Original): A microcomputer formed on single chip, including						
2	memory storing M-bit instructions and N-bit instructions where M and N are						
3	integers, and N is greater than M;						
4	a translator coupled to the memory to receive M-bit instructions for translation of						
5	each received M-bit instruction to a sequence of one or more N-bit instructions; and						
6	a decoder coupled to the memory and to the decoder for receiving and decoding						
7	the N-bit instructions.						
1	15. (Canceled)						
1	16. (Original): The microcomputer of claim 14, where the N-bit instructions						
2	include an N-bit branch instruction that contains data indicative of a branch address of a target						
3	instruction, the branch address having a bit position set to a first state when the target instruction						
4	is an M-bit instruction.						
1	17. (Original): A method of executing M -bit instructions and N-bit						
2	instructions by a microcomputer formed on a single chip, M and N being integers, and M is less						
3	than N, the method including the steps of:						

Appl. No. Unassigned Amdt. dated August 19, 2003 Preliminary Amendment

4	storing the M-bit and N-bit instructions in a memory;						
5	operating in a first mode to sequentially decode ones of the N-bit instructions;						
6	operating in a second mode to sequentially translate ones of the M-bit instructions						
7	to a sequence of one or more N-bit instructions, and then decoding the N-bit instructions.						
1	18. (Original): The method of claim 17, wherein the N-bit instructions						
2	include an N-bit branch instruction, and the step of operating in the first mode includes decoding						
3	the N-bit branch instruction to branch to an M-bit instruction having a memory address with a						
4	least significant bit set to a first state to switch from the first state to the second state of						
5	operation.						
1	19. (Original): In a microcomputer structured to execute N-bit instructions,						
2	including an N-bit branch instruction, and M-bit instructions, including an M-bit branch						
3	instruction, where M and N are integers, and N is greater than M, a method of executing the M-						
4	bit instructions that includes the steps of:						
5	emulating each of the M-bit branch instructions with a sequence of one or more						
6	N-bit instructions;						
7	emulating the M-bit branch instruction with a prepare to branch instruction that						
8	provides a branch address and thereafter the N-bit branch instruction that uses the branch						
9	address.						
1	20. (Original): The method of claim 19, including the step of providing at						
2	least one target address register, and the step of emulating the M-bit branch instruction includes						
3	the prepare to branch instruction loading the target address register with the target address.						
1	21. (Original): The method of claim 20, the step of emulating the M-bit						
2	branch instruction including the step of the N-bit branch instruction reading the target address fo						
3	the target address.						

1		22.	(Original):	The microcomputer of claim 14, including a plurality of		
2	general purpose registers each for storing data in response to one or more of the N-bit					
3	instructions.					
1		23.	(Original):	The microcomputer of claim 22, wherein the plurality of		
2	general purpose registers each includes 2N bit positions.					
1		24.	(Canceled)			
1		25.	(Original):	The microcomputer of claim 22, wherein first ones of the one		
2	or more N-bit instructions load data in low-order bit positions of selected one of the plurality of					
3	general purpose registers, and second ones of the one or more N-bit instructions load data in					
4	high-order bit positions of the plurality of general purpose registers.					
1		26.	(Canceled)			